UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,054	09/15/2000	Randy M. Bonella	10559/350001/P10068	4989

20985 7590 07/19/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	13

DATE MAILED: 07/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/662,054	Applicant(s) BONELLA ET AL.	
	Examiner Dennis M. Butler	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8,9,11,12,22-25,27-41,46 and 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8,9,11,12,22-25,27-41,46 and 47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the RCE filed on June 16, 2004. Claims 1-4, 8-9, 11-12, 22-25, 27-41 and 46-47 are pending.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 22-25, 27-32 and 40-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 22, the phrase "said system crash" lacks proper antecedent basis.

Claims 23-25 and 27-32 are rejected because they incorporate the deficiencies of claim 22.

Claim 28 is unclear as to whether it further limits claim 25 because claim 22 already seems to recite that a system event is a system crash.

Regarding claim 29, the phrase "said reobtaining" lacks proper antecedent basis.

Regarding claims 40 and 41, the phrase "said system event" lacks proper antecedent basis.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

> 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-4, 9, 12, 33, 35 and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Coteus et al., U. S. Patent 6,292,903.

Per claims 1-4, 9, 12, 33, 35 and 46:

Coteus et al teach the claimed items including a data source having a plurality of different lines (Memory Controller 1 and/or DIMMs 14a-14n, Data In lines 104a-n and Data lines 105a-n of figures 2a and 2b), a plurality of programmable delay elements each coupled to one of the lines (Flip-Flops 10a2a-10a2n, Flip-Flops 10a3a-1-a3n and Delays 15a-15n and 16a-16n of figures 2A and 2B and figure

9a), storing values for the programmable delay elements in a register (Memory 3 of figure 1 and Delay Value Info of figure 2b), determining if a system event has occurred (system power-up of figure 3a), arbitration logic having first and second elements (microprocessor 2 and the operating program in memory 3) and testing the signals for the proper delay values (figures 3a-3f) at column 6, line 33 – column 8, line 30, at column 10, lines 10-16, at column 24, line 66 – column 25, line 10 and at column 25, line 65 – column 26, line 8.

8. Claims 22-23, 25, 27-32, 37-41 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al., U. S. Patent 6,292,903 in view of Mueller, Upgrading and Repairing PCs.

Per claims 22-23, 25, 28-30 and 37-39:

A) Coteus et al teach the claimed items including a data source having a plurality of different lines (Memory Controller 1 and/or DIMMs 14a-14n, Data In lines 104a-n and Data lines 105a-n of figures 2a and 2b), a plurality of programmable delay elements each coupled to one of the lines (Flip-Flops 10a2a-10a2n, Flip-Flops 10a3a-1-a3n and Delays 15a-15n and 16a-16n of figures 2A and 2B and figure 9a), storing values for the programmable delay elements in a register (Memory 3 of figure 1 and Delay Value Info of figure 2b), determining if a system event has occurred (system power-up of figure 3a), arbitration logic having first and second elements (microprocessor 2 and the operating program in memory 3) and testing the signals for the proper delay values (figures 3a-3f) at column 6, line 33 – column 8, line 30, at column 10, lines

10-16, at column 24, line 66 – column 25, line 10 and at column 25, line 65 – column 26, line 8.

B) The claims seem to differ from Coteus in that Coteus fails to explicitly teach determining and applying/storing new delay values in response to detecting a system crash as claimed.

C) However, Coteus describes determining if a power up event has occurred with detecting or determining the system power-up of figure 3a, at column 10, lines 10-21 and at column 24, line 66 – column 25, line 10. Coteus clearly describes an event detector (microprocessor 2) and determining new delay values each time a power up event occurs (figure 3). Therefore, Coteus discloses the claimed invention except for explicitly reciting that the event is a system crash. However, it is well known in the art to re-power the system when a system crash occurs. Normally when a system crashes it stops operating and the only option a user has is to turn the power off and re-power the system. Coteus describes determining new delay values each time a power up event occurs (figure 3). Furthermore, Mueller teaches that it is known to re-power a system when it crashes in order to run the POST to test and troubleshoot the system at page 835 through page 837. Mueller describes that the POST operates whenever a PC is powered up or turned on and that operators often use the POST to test and troubleshoot most systems. It would have been obvious to one having ordinary skill in the art at the time the invention was made to determine and apply/store new delay values in response to detecting a system crash, as

suggested by Coteus in view of Mueller, in order to reprogram the programmable delays with optimized settings for receiving, latching or transmitting data. One of ordinary skill in the art would have been motivated to combine Coteus and Mueller because of Mueller's teaching that it is well known to power up a system when the system is not operating properly in order to use the POST to test and troubleshoot the system at the top of page 836. It would have been obvious for one of ordinary skill in the art to combine Coteus and Mueller because Mueller teaches what is already well known in the art and Coteus testing and reprogramming of the programmable delays during power up acts as an extension of the booting POST testing and initialization process.

Per claims 27, 31-32, 40, 41 and 47:

Coteus does not explicitly describe the system event including a system component change or an operating system crash. However, as described above, Coteus describes the system event including a power up initialization event with figure 3a. It is well known to re-power and initialize the system when either a system component change or an operating system crash occurs. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to cause the system to be re-powered and initialized when either a system component change or an operating system crash occurs in order to recognize and initialize the component change, re-install the operating system and redetermine and reprogram the delay values in the programmable delays.

Coteus describes programmably delaying signals such that the signals are latched or loaded into a flip flop during an enablement period during a positive edge of a clock signal at column 6, lines 33-67. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the minimal delay required or to delay signals such that they a skewed relative to a clock margin of a system in order to allow for clock skew and reliably latch or load the signals into flip flops using the clock.

9. Claims 8, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al., U. S. Patent 6,292,903 in view of Huang et al., U.S. Patent 6,041,419.

Per claims 8 and 34:

Coteus does not explicitly describe that the signals are from a graphics device as claimed. However, Huang describes that it is known in the graphics processing art that graphics devices transmit signals that require synchronization by using programmable delay devices in order to properly sample the signals with figures 1 and 6, at column 1, lines 12-46 and at column 3, line 21 – column 4, line 14. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Coteus's smart memory interface in a graphics processing system in order to align the clock and data signals transmitted in the graphics processing system for proper sampling of the data signals. One of ordinary skill in the art would have been motivated to combine Coteus and Huang because of Coteus's suggestion of synchronizing signals in memory subsystems

at column 1, line 65 – column 2, line 26. It would have been obvious for one of ordinary skill in the art to combine Coteus and Huang because they are both directed to the problem of synchronizing data and clock signals in memory subsystems.

10. Claims 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al., U. S. Patent 6,292,903 in view of Mueller, Upgrading and Repairing PCs and further in view of Huang et al., U.S. Patent 6,041,419.

Per claim 24:

Coteus does not explicitly describe that the signals are from a graphics device as claimed. However, Huang describes that it is known in the graphics processing art that graphics devices transmit signals that require synchronization by using programmable delay devices in order to properly sample the signals with figures 1 and 6, at column 1, lines 12-46 and at column 3, line 21 – column 4, line 14. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Coteus's smart memory interface in a graphics processing system in order to align the clock and data signals transmitted in the graphics processing system for proper sampling of the data signals. One of ordinary skill in the art would have been motivated to combine Coteus and Huang because of Coteus's suggestion of synchronizing signals in memory subsystems at column 1, line 65 – column 2, line 26. It would have been obvious for one of ordinary skill in the art to combine Coteus and Huang because they are both

directed to the problem of synchronizing data and clock signals in memory subsystems.

11. Claims 11 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al., U. S. Patent 6,292,903 in view of Jeddeloh, U.S. Patent 6,629,222.

Per claim 11:

Jeddeloh describes that it is known to store a delay value that produces a best desired result that is one where a plurality of delayed signals are received at substantially the same time with figures 4 and 6, at column 6, lines 9-16 and at column 7, lines 5-23. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store a delay value that produces a best desired result in order to determine the best desired result delay value directly without performing a calculation. One of ordinary skill in the art would have been motivated to combine Coteus and Jeddeloh because of Coteus's suggestion of synchronizing signals in memory subsystems at column 1, line 65 – column 2, line 26. It would have been obvious for one of ordinary skill in the art to combine Coteus and Jeddeloh because they are both directed to the problem of synchronizing data and clock signals in memory subsystems.

Per claim 36:

Coteus describes programmably delaying signals such that the signals are latched or loaded into a flip flop during an enablement period during a positive edge of a clock signal at column 6, lines 33-67. It would have been obvious to one having ordinary skill in the art at the time the invention was made to delay

signals such that they a skewed relative to a clock margin of a system in order to reliably latch or load the signals into flip flops using the clock.

12. Applicant's arguments filed on May 21, 2004 have been fully considered but they are not persuasive.

In the Remarks, applicant has argued in substance that:

A. Claim 1 requires that the arbitration logic checks different set of values to determine which set produces the best result.

B. Coteus increments through delays until a desired delay amount is obtained. There is no teaching or suggestion of storing multiple different sets of delay values and testing each of these sets to use the one which obtains the optimum delay set.

C. Coteus alone or in view of Jeddeloh does not teach detecting new delay values when a specified event occurs or responsive to a system crash.

D. Claim 33 defines different sets of values that are not taught or suggested by Coteus. At best, Coteus teaches only one set of values not finding a best one among multiple sets.

13. As to point A, the examiner disagrees with applicant's contention. Coteus clearly describes arbitration logic that checks different sets of values to determine the one set that produces the best result as described in the above rejection. Figures 3e and 3f show values that produce the best result being stored as flag 16a1 and/or 16a2. Coteus describes that each of the plurality of delays 11a, 15a through 15n and 16a through 16n are programmable through the corresponding inputs 11a', 15a-n' and 16a-n' as shown

in figures 2a and 2b. Coteus describes that each of the plurality of delays has at least ten increments of delay and the amount (increment) of delay is programmed or set using the values shown in figure 2c. Coteus describes that each of the plurality of delays has a corresponding delay value that is stored in memory 3 as a flag variable as shown in figures 1 and 2b and as described in the above rejection. Coteus further describes that component block 110a of figures 2a and 2b that contains the plurality of delays is just one of n component blocks in the memory controller. Each component block contains a plurality of delays that all have corresponding delay values. The collection of delay values comprising the present delay values being used by the programmable delays corresponds to a set. When at least one of the delay values of the present set changes, a new set is produced. Coteus describes that the arbitration logic increments the delay value for a programmable delay until the value that produces the optimum result is determined. This is done for each of the plurality of programmable delays. Therefore, each time at least one delay value is changed, a new set is produced. The arbitration logic of Coteus clearly checks different set of delay values in order to determine the set that produces the best result as recited in claim 1.

As to point B, the examiner disagrees with applicant's contention. Claim 1 does not recite storing multiple different sets of delay values and testing each of these sets. Claim 1 recites that a first element produces a set of first values and that arbitration logic dithers between different sets of values. Applicant's specification defines dithering as "adding a certain amount of delay amount" at page 6, lines 13-14. These storing limitations are not in the claim. Therefore, it is irrelevant whether Coteus teaches storing

multiple different sets of values and testing each set of values. Applicant has repeatedly made the above assertion that the claims recite the limitation of storing multiple different sets of delay values and testing each of these sets even after the examiner pointed out that these limitations are not recited in the claims. The examiner has reviewed applicant's claims and again cannot find this limitation recited in any of the claims. In addition, the examiner has reviewed applicant's specification and could not find any description of storing multiple different sets of delay values and testing each of these sets in the specification. Applicant is requested to specifically point out where in the claims the limitation storing multiple different sets of delay values and testing each of these sets is recited in the claims and where support is provided for this limitation in the specification. At this point, the examiner does not consider this limitation to be part of applicant's invention and will not respond to further arguments directed to this limitation unless applicant can point to the limitation in the claims and where it is supported in the specification. Claim 1 does not recite obtaining the set that works best as the optimum delay set. Claim 1 merely recites storing the plurality of values that produce a best desired result. Therefore, it is irrelevant whether Coteus teaches this feature.

As to point C, the examiner has fully addressed these issues in the above rejection of claims 22-23, 25, 28-30 and 37-39.

As to point D, the examiner disagrees with applicant's contention. Coteus clearly describes providing different sets of values. Coteus describes that each of the plurality of delays 11a, 15a through 15n and 16a through 16n are programmable through the corresponding inputs 11a', 15a-n' and 16a-n' as shown in figures 2a and 2b. Coteus

describes that each of the plurality of delays has at least ten increments of delay and the amount (increment) of delay is programmed or set using the values shown in figure 2c. Coteus describes that each of the plurality of delays has a corresponding delay value that is stored in memory 3 as a flag variable as shown in figures 1 and 2b and as described in the above rejection. Coteus further describes that component block 110a of figures 2a and 2b that contains the plurality of delays is just one of n component blocks in the memory controller. Each component block contains a plurality of delays that all have corresponding delay values. The collection of delay values comprising the present delay values being used by the programmable delays corresponds to a set. When at least one of the delay values of the present set changes, a new set is produced. Coteus describes that the arbitration logic increments the delay value for a programmable delay until the value that produces the optimum result is determined. This is done for each of the plurality of programmable delays. Therefore, a new set is produced each time at least one delay value is changed. The arbitration logic of Coteus clearly provides different set of delay values in order to determine the set that produces the best result as recited in claim 33.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler
Primary Examiner
Art Unit 2115